

1. (Currently amended) A system [[System]] for driving columns of a liquid crystal display comprising:

[[a]] logic circuitry [[(10)]] operating in a supply path between a first [[(VDD)]] and a second [[(VSS)]] supply voltage with said first supply voltage [[(VDD)]] higher than said second supply voltage [[(VSS)]], said logic circuitry [[(10)]] being capable of generating [[starting from the]] first logic signals [[(LOW_FRAME, WHITE_PIX) in input]] and second logic signals [[(CP, CN, CP_N, CN_N) in output]] whose value is equal to said first [[(VDD)]] or second [[(VSS) supply voltage,]];:

elevator devices [[(11, 12)]] coupled to said logic circuitry [[(10)]] and operating in a supply path between a third supply voltage [[(VLCD)]] greater than said first supply voltage [[(VDD)]] and said second supply voltage [[(VSS)]], said elevator devices [[(11, 12)]] being capable of raising the value of said second logic signals [[(CP, CN, CP_N, CN_N,)];:

a first [[(T11-T12)]] and a second [[(T13-T14)]] pair of transistors having different supply paths [[(VLCD-VA, VB-VSS)]] and having an output terminal [[(OUT)]] in common, said first [[(T11-T12)]] and second [[(T13-T14)]] pair of transistors being associated with [[to]] said elevator devices [[(11, 12)]] and [[a]] said logic circuitry [[(10) so as]] to determine the drive signal of a column, wherein [[characterised in that]] said elevator devices [[(11, 12)]] are [[two and each of them is]] coupled to [[connected with]] one of said pairs of transistors [[(T11-T12, T13-T14,)]; and

[[in that it comprises]] turnoff circuitry [[(15)]] coupled to said [[two]] elevator devices [[(11, 12)], said turnoff circuitry [[(10)]] being capable of keeping one of said two pairs of transistors [[(T11-T12, T13-T14)]] in the turnoff state in the period of time of a frame when the other of said two pairs of transistors [[(T11-T12, T13-T14)]] is [[in]] operative [[conditions]].

2. (Currently amended) The system [[Device]] according to claim 1, wherein [[characterised in that]] said turnoff circuitry [[(15)]] operates in a supply path between said third [[(VLCD)]] and said second supply voltage [[(VSS)]].

3. (Currently amended) The system [[Device]] according to claim 1, wherein [[characterised in that]] each of said [[two]] elevator devices [[(11, 12)]] separately drives [[separately]] the transistors of one of said pairs [[(T11-T12,

T13-T14))] of transistors.

4. (Currently amended) The system [[Device]] according to claim 3, wherein [[characterised in that]] said turnoff circuitry [[(15) has]] one [[(LOW_FRAME)]] of said first logic signals [(LOW_FRAME, WHITE_PIX) in input whose value]] changes value in response [[according]] to an even frame or an uneven frame.

5. (Currently amended) The system [[Device]] according to claim 4, wherein [[characterised in that]] said turnoff circuitry [[(15)]] sends two signals [(tr_state1, tr_state2)] complementary with each other respectively to said [[two]] elevator devices [(11, 12)] according to the state of one of said first logic signals [[signal (LOW_FRAME) in input so as]] to inhibit the turning on of one of or the other elevator devices [[device]].

6. (Currently amended) The system [[Device]] according to claim 5, wherein [[characterised in that]] said pairs of transistors [(T11-T12, T13-T14) are]] comprise pairs of MOS transistors [[MOS]].

7. (Currently amended) They system [[Device]] according to claim 6, wherein [[characterised in that]] said pairs of MOS transistors [[MOS (T11-T12, T13-T14) are made up of]] comprise a pair of PMOS transistors [[PMOS (T11-T12)]] and of a pair of NMOS transistors [[NMOS (T13-T14)]], and said [[two]] elevator devices [(11, 12)] each comprise a first [(M8, M14)] and a second [(M9, M15)] NMOS transistor [[NMOS]] driven by two of said second logic signals [(CP, CN, CP_N, CN_N)] complementary between each other and a first [(M4, M12)] and a second PMOS [(M5, M13)] transistor [[PMOS]] having the terminals that can be driven coupled [[connected]] respectively with the drain terminal of said second [(M9, M15)] and first [(M8, M14) transistor NMOS]] NMOS transistors, the drain terminals coupled [[connected]] respectively with the drain terminals of said first [(M8, M14)] and second [(M9, M15) transistor NMOS]] NMOS transistors, and the source terminals coupled to [[with]] said third supply voltage [(VLCD)].

8. (Currently amended) The system [[Device]] according to claim 7, wherein [[characterised in that]] said turnoff circuitry [(15)] comprises a first

transistor [(M7) on whose] having a gate terminal [(that can be)] driven by said one of first logic signals [(signal (LOW_FRAME) in input is present)] and having a first non-driven terminal coupled [(that cannot be driven connected)] to said second supply voltage [(VSS)] and a second non-driven [(the other)] terminal [(that cannot be driven connected)] coupled to non-driven [(the)] terminals [(that can be driven)] of two additional transistors [(M3, M6)] having a first non-driven terminal coupled [(terminals that cannot be driven connected)] respectively with the drain terminals of said first [(M8)] and second [(M9)] NMOS transistor [(NMOS)] of one [(11)] of said elevator devices [(11, 12)] and a second non-driven [(the other)] terminal [(that cannot be driven connected with)] coupled to said third supply voltage [(VLCD)], the non-driven terminal [(that can be driven)] of said two additional transistors [(M3, M6)] being coupled [(connected)] to the non-driven terminal [(that can be driven)] in common with two more additional transistors [(M10, M11)] having first non-driven terminals [(that cannot be driven connected)] respectively coupled to [(with)] the source terminals of said first [(M12)] and second [(M13)] PMOS transistor [(PMOS)] of one of [(the other of (12))] said elevator devices [(11, 12)] and the other non-driven terminal [(that cannot be driven connected)] coupled to the third supply voltage [(VLCD)], said turnoff circuitry [(15)] comprising two more additional transistors [(M1, M2)] having non-driven [(the)] terminals [(that can be driven connected)] respectively coupled to [(with)] the drain terminals of said first [(M8)] and second [(M9)] NMOS transistor [(NMOS)] of one [(11)] of said elevator devices [(11, 12)], first non-driven terminals [(that cannot be driven connected)] coupled to said additional non-driven terminal [(that cannot be driven)] of said first transistor [(M7)] and second non-driven terminal [(that cannot be driven connected)] coupled to said third supply voltage [(VLCD)].